This listing of the claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF THE CLAIMS:

1-15. (Cancelled).

16. (Currently Amended) A MOSFET device comprising a silicon substrate having shallow trench isolation STI and source and drain regions located therein, a gate dielectric and a gate stack located on said silicon substrate between the source and drain regions, and a fluorine doped low K dielectric oxide gate spacers located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2}, wherein ~~the~~ said fluorine doped low K dielectric oxide gate spacer is in direct contact with an overlying silicon nitride oxide layer and at least a portion of said source and drain regions ~~are essentially free of fluorine~~ directly contacts said silicon nitride oxide layer.

17. (Previously Presented) The MOSFET device of Claim 16 wherein said fluorine doped low K dielectric oxide gate spacer has a dielectric constant value in a range of 3.3 to 4.0.

18. (Previously Presented) The MOSFET device of Claim 16 wherein said fluorine doped low K dielectric oxide gate spacer has a dielectric constant value of substantially 3.3.

19. (Cancelled).

20. (Currently Amended) The MOSFET device of Claim 16 ~~further comprising a~~ wherein said silicon nitride oxide layer ~~located on at least~~ overlays said gate stack.

21. (Currently Amended) A MOSFET device comprising a silicon substrate having shallow trench isolation (STI) located therein, a gate dielectric and a gate stack located on said silicon substrate, a fluorine doped low K dielectric oxide gate spacer located on sidewalls of said gate stack, and a silicon nitride oxide layer overlaying and contacting said gate stack, said fluorine doped low K dielectric oxide gate spacer, and remaining surfaces of the silicon substrate, wherein no material with a dielectric constant greater than 4.0 is present between said fluorine doped low K dielectric oxide gate spacer and said silicon nitride oxide layer.